What is claimed is:

[Claim 1] A method of forming an integrated circuit structure in a structure layer disposed above a substrate comprising the steps of:

Forming a hardmask layer disposed above said structure layer;
Forming a protective layer above said hardmask layer;
Forming a temporary layer above said protective layer;
Patterning said temporary layer in a set of pillars in positions related to positions of said structures;
Forming a conformal layer over said set of pillars, said conformal layer having a top portion on top of said pillars, sidewalls adjacent to sides of said set of pillars and a horizontal portion extending between members of said set of pillars and disposed directly on top of said protective layer;
Removing at least said top portion of said conformal layer;
Removing said set of pillars, whereby said protective layer in locations beneath said set of pillars is exposed;
Etching said protective layer, using said sidewalls as a mask, thereby defining a first set of hardmask regions in said protective layer;
Etching said hardmask layer using said first set of hardmask regions in said protective layer as hardmask, thereby defining a second set of hardmask in said hardmask layer that are symmetric on opposite sides of said sidewalls; and
Etching said structure layer using said second set of hardmask, thereby forming said structures.

[Claim 2] A method according to claim 1, in which a further step comprises depositing and patterning a block mask that exposes selected members of said set of hardmask regions and stripping said hard mask regions selective to said structure layer, thereby changing the number of hardmask regions.

[Claim 3] A method according to claim 1, in which a further step strips said sidewalls and said first set of hardmask, before said step of etching said structure layer.

[Claim 4] A method according to claim 2, in which a further step strips said sidewalls and said first set of hardmask, before said step of etching said structure layer.

[Claim 5] A method according to claim 1, in which said structure layer is silicon, said hardmask layer is oxide and said protective layer is nitride.

[Claim 6] A method according to claim 5, in which said substrate is an SOI silicon substrate.

[Claim 7] A method according to claim 5, in which said substrate is a bulk silicon substrate.

[Claim 8] A method according to claim 1, in which said structure layer is silicon-germanium alloy, said hardmask layer is oxide and said protective layer is nitride.

[Claim 9] A method according to claim 8, in which said substrate is silicon with a layer of buried insulator separating said substrate from said structure layer.

[Claim 10] A method according to claim 8, in which said substrate is a bulk silicon substrate with a structure layer of Silicon-Germanium alloy formed on a top surface thereof.

[Claim 11] A method of forming an integrated circuit structure in a structure layer disposed above a substrate comprising the steps of:

Forming a hardmask layer disposed above said structure layer;
Forming a protective layer above said hardmask layer;
Forming a temporary layer above said protective layer;
Patterning said temporary layer in a set of pillars in positions related to positions of said structures;
Forming a first conformal layer over said set of pillars, said first conformal layer having a top portion on top of said pillars, first sidewalls adjacent to sides of said set of pillars and a first horizontal portion extending between members of said set of pillars and disposed directly on top of said protective layer;
Removing at least said top portion of said first conformal layer;
Removing said set of pillars, thereby defining a first set of sidewalls;
Depositing a second conformal layer over said first set of sidewalls;
Removing at least said top portion of said second conformal layer;
Removing said first set of sidewalls, thereby defining a second set of sidewalls formed from said second conformal layer, whereby said protective layer in locations beneath said first set of sidewalls is exposed;

Etching said protective layer, using said second set of sidewalls as a mask, thereby defining a first set of hardmask regions in said protective layer;
Etching said hardmask layer using said first set of hardmask regions in said protective layer as hardmask, thereby defining a second set of hardmask in said hardmask layer that are symmetric on opposite sides of said sidewalls; and
Etching said structure layer using said second set of hardmask, thereby forming said structures.

[Claim 12] A method according to claim 11, in which a further step comprises depositing and patterning a block mask that exposes selected members of said set of hardmask regions and stripping said hard mask regions selective to said structure layer, thereby changing the number of hardmask regions.

[Claim 13] A method according to claim 11, in which a further step strips said second set of sidewalls and said first set of hardmask, before said step of etching said structure layer.

[Claim 14] A method according to claim 12, in which a further step strips said second set of sidewalls and said first set of hardmask, before said step of etching said structure layer.

[Claim 15] A method according to claim 11, in which said structure layer is silicon, said hardmask layer is oxide and said protective layer is nitride.

[Claim 16] A method according to claim 15, in which said substrate is an SOI silicon substrate.

[Claim 17] A method according to claim 15, in which said substrate is a bulk silicon substrate.

[Claim 18] A method according to claim 11, in which said structure layer is silicon-germanium alloy, said hardmask layer is oxide and said protective layer is nitride.

[Claim 19] A method according to claim 18, in which said substrate is silicon with a layer of buried insulator separating said substrate from said structure layer.

[Claim 20] A method according to claim 18, in which said substrate is a bulk silicon substrate with a structure layer of Silicon-Germanium alloy formed on a top surface thereof.